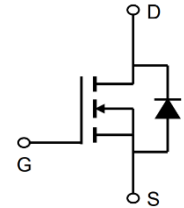


### Description

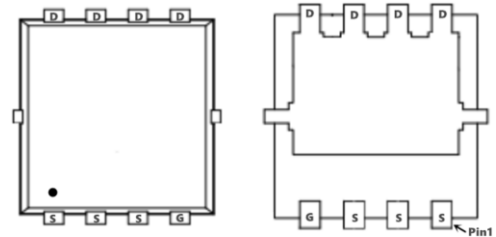
The LMP3065BQU uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 30V$   $I_D = 65A$

$R_{DS(ON)} < 7m\Omega$  @  $V_{GS}=10V$



### Application

- Lithium battery protection
- Wireless impact
- Mobile phone fast charging



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
LMP3065BQU	PDFN3*3	AP65N03DF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	65	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	24	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	15	A
IDM	Pulsed Drain Current <sup>2</sup>	100	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	28.8	mJ
IAS	Avalanche Current	24	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	24	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	60	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	5.2	$^\circ C/W$

## Electrical Characteristics ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	37	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=20A$	---	5	7	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$	---	6.9	9	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	43	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.7	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	8	---	nC
$Q_{gs}$	Gate-Source Charge		---	2.4	---	
$Q_{gd}$	Gate-Drain Charge		---	3.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	7.1	---	ns
$T_r$	Rise Time		---	40	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15	---	
$T_f$	Fall Time		---	6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	814	---	pF
$C_{oss}$	Output Capacitance		---	498	---	
$C_{rss}$	Reverse Transfer Capacitance		---	41	---	
$I_S$	Continuous Source Current <sup>1,6</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	24	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1	V
$t_{rr}$	Reverse Recovery Time	$I_F=15A, di/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	---	34	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	15	---	nC

### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、 The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=24A$
- 4、 The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 5、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

## Typical Characteristics

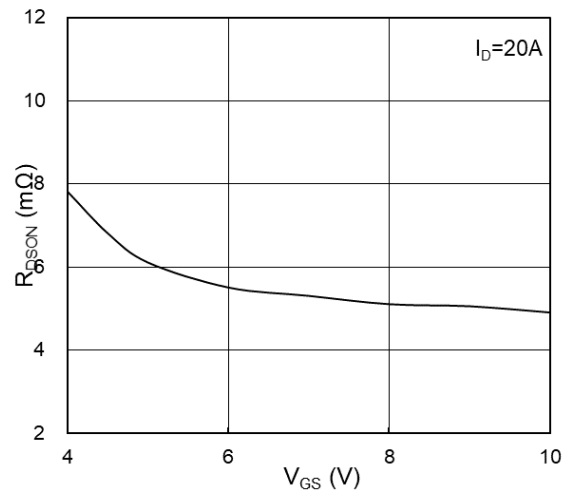
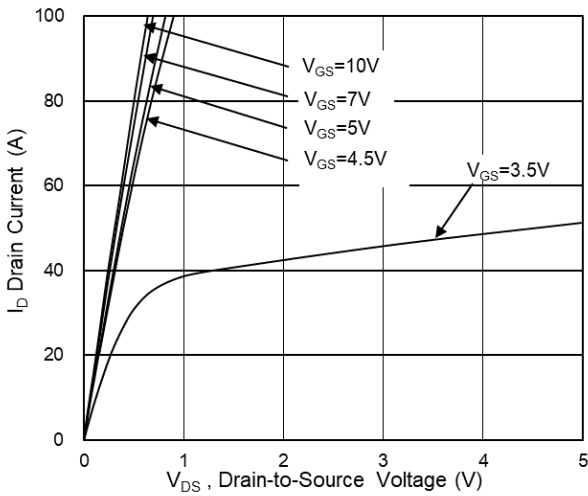


Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs G-S Voltage

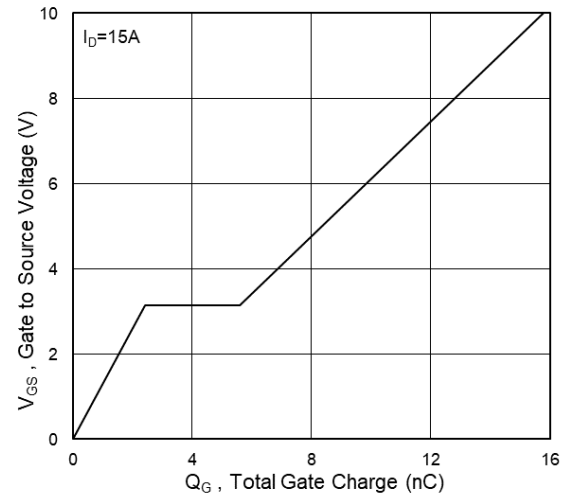
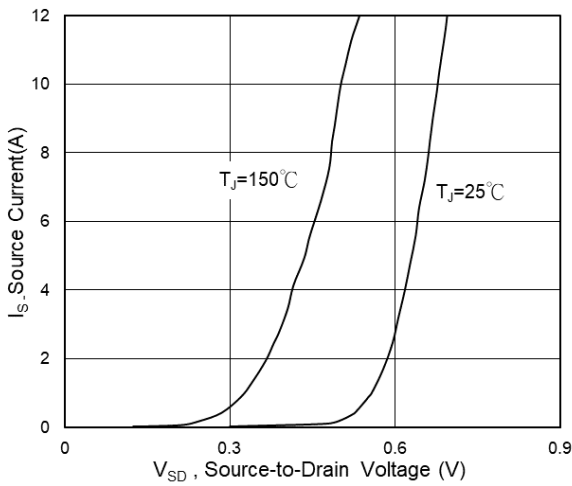


Fig.3 Source Drain Forward Characteristics

Fig.4 Gate-Charge Characteristics

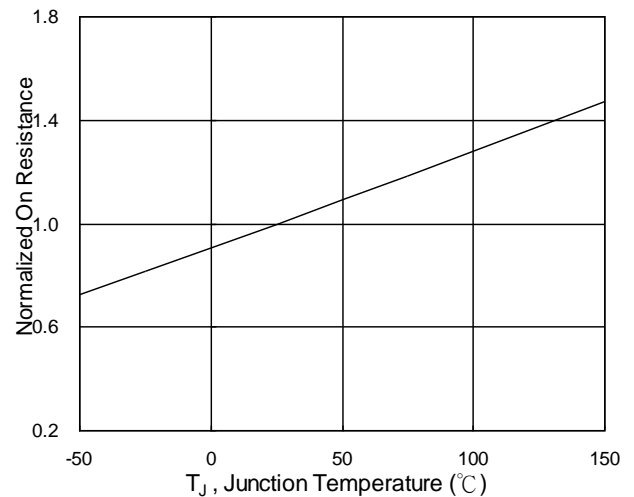
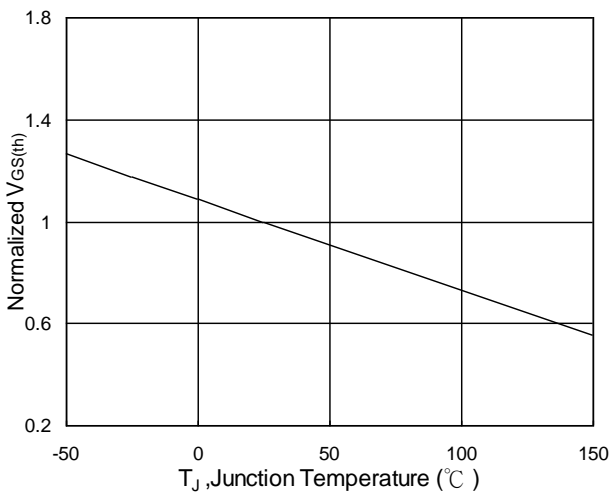
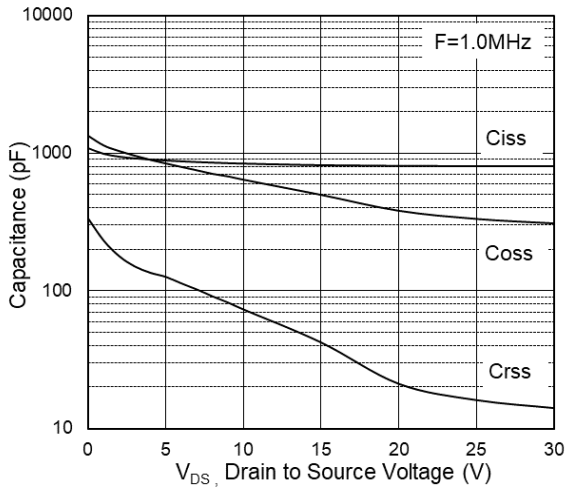
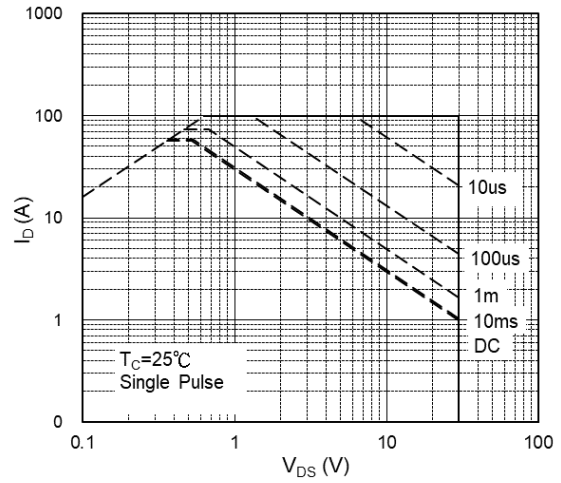


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

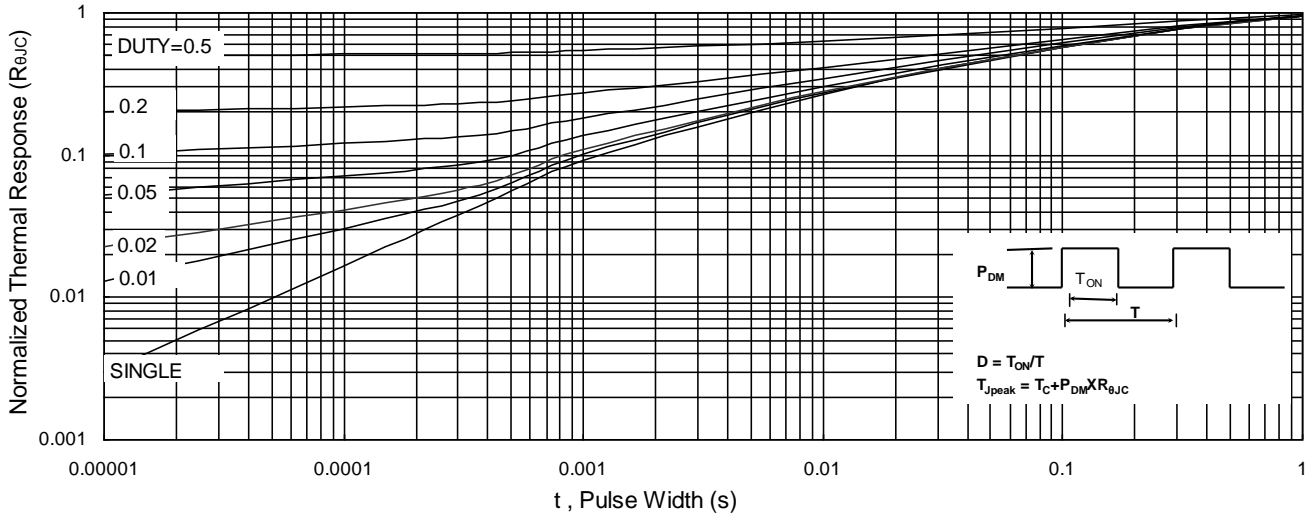
Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$



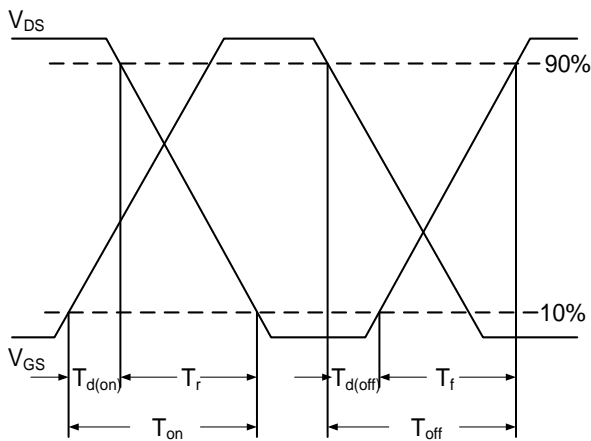
**Fig.7 Capacitance**



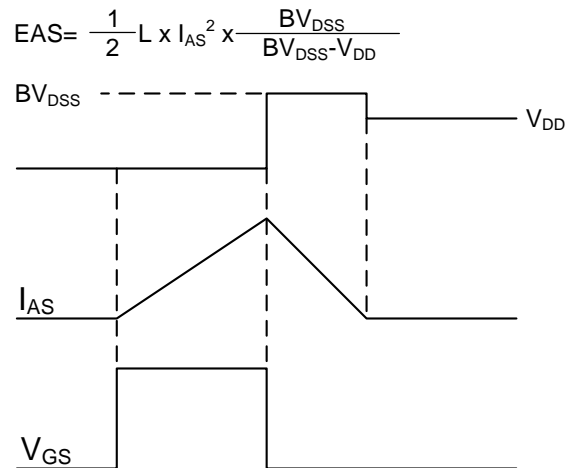
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

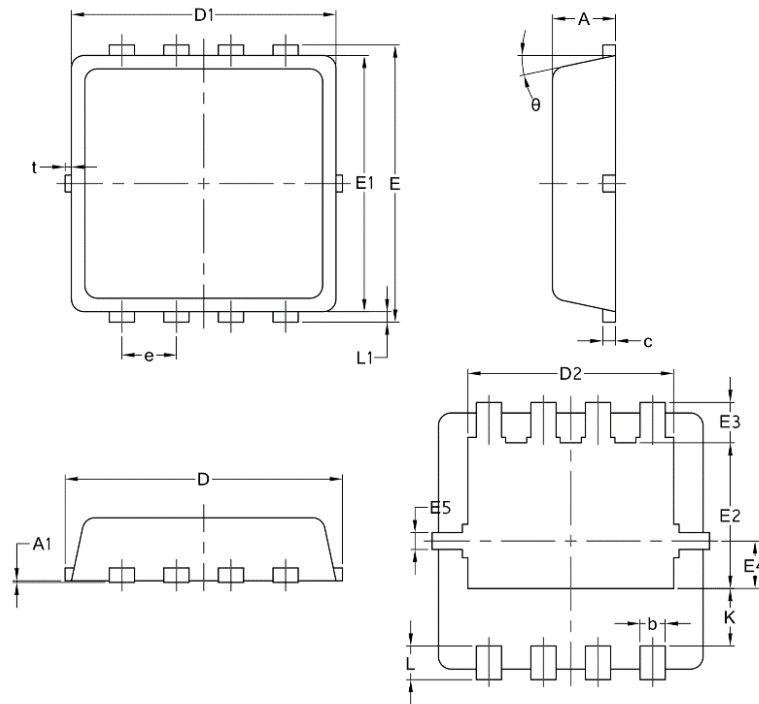


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

## Package Mechanical Data-DFN3\*3 Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
$\Phi$	10	12	14

Shanghai Leiditech Electronic Co.,Ltd  
 Email: sale1@leiditech.com  
 Tel : +86- 021 50828806  
 Fax : +86- 021 50477059