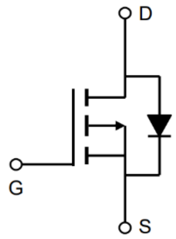
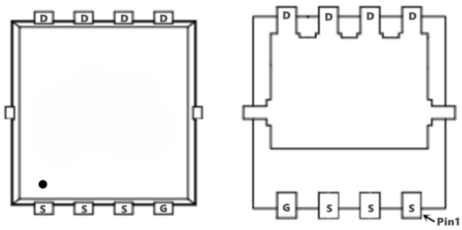
LM5D50P03

30V P-Channel Enhancement Mode MOSFET

Description

The LM5D50P03 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = -30V I_D =-50A

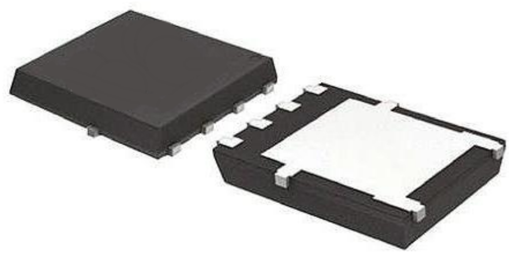
$R_{DS(ON)}$ < 13mΩ @ V_{GS}=-10V

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



Package Marking and Ordering Information

Device	Device Marking	Device Package	Reel Size	Tape width	Quantity
LM5D50P03	AP50P03NF	DFN5X6-8	-	-	5000 units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±25	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-50	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-30	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-9.6	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -10V[1]	-7.7	A
I_{DM}	Pulsed Drain Current[2]	-150	A
EAS	Single Pulse Avalanche Energy[3]	125	mJ
I_{AS}	Avalanche Current	-50	A
P_D@T_C=25℃	Total Power Dissipation[4]	45	W
P_D@T_A=25℃	Total Power Dissipation[4]	2.0	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62	℃/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1] (t ≤10s)	25	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.8	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	-33	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.0232	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-12A	---	9	13	mΩ
		V_{GS}=-4.5V , I_D=-8A	---	14	20	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.7	-2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±25V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-30A	---	30	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	9	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-15A	---	22	---	nC
Qgs	Gate-Source Charge		---	8.7	---	
Qgd	Gate-Drain Charge		---	7.2	---	
Td(on)	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω I_D=-15A	---	8	---	ns
T_r	Rise Time		---	73.7	---	
Td(off)	Turn-Off Delay Time		---	61.8	---	
T_f	Fall Time		---	24.4	---	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	2215	---	pF
Coss	Output Capacitance		---	310	---	
Crss	Reverse Transfer Capacitance		---	237	---	
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-45	A
ISM	Pulsed Source Current[2,5]		---	---	-150	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
trr	Reverse Recovery Time	IF=-15A , dI/dt=100A/μs , T_J=25℃	---	19	---	nS
Q_{rr}	Reverse Recovery Charge		---	9	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-50A
4.The power dissipation is limited by 150°C junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Electrical and Thermal Characteristics

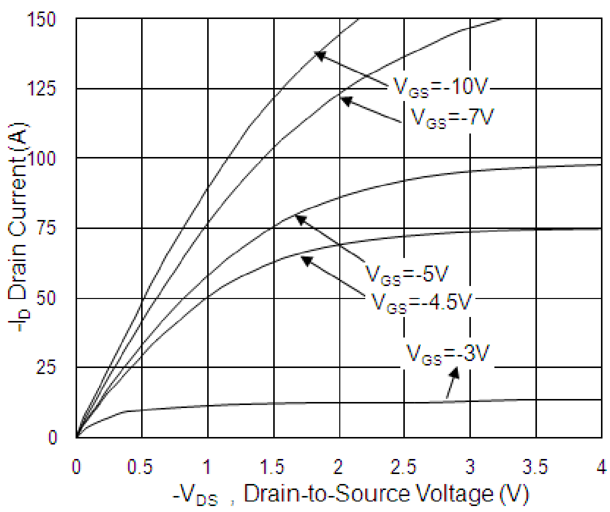


Fig.1 Typical Output Characteristics

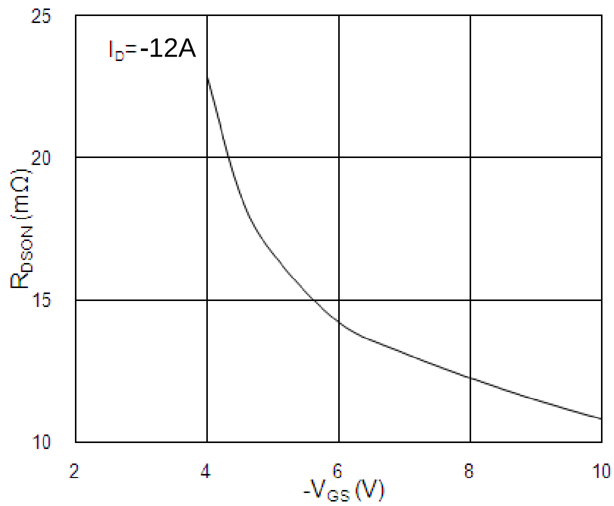


Fig.2 On-Resistance vs. G-S Voltage

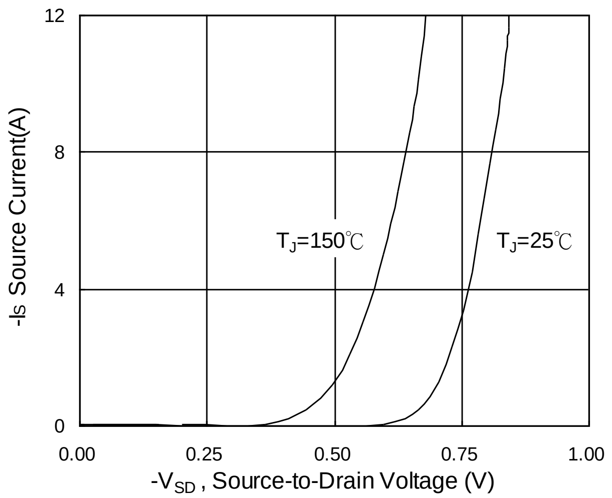


Fig.3 Forward Characteristics of Reverse

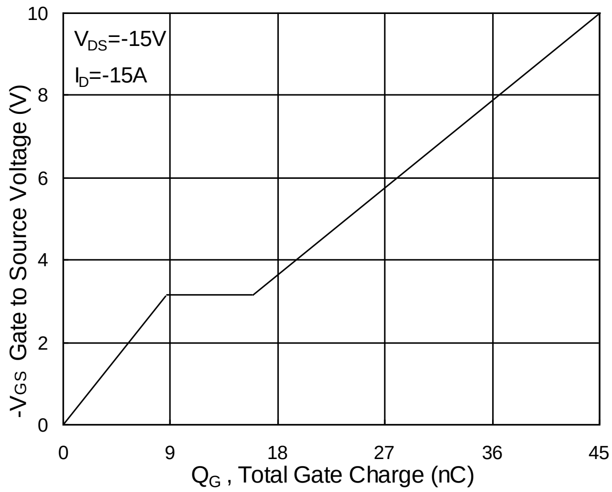


Fig.4 Gate-charge Characteristics

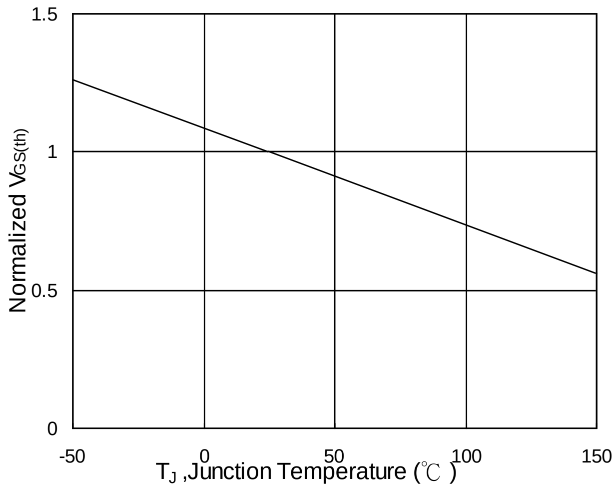


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

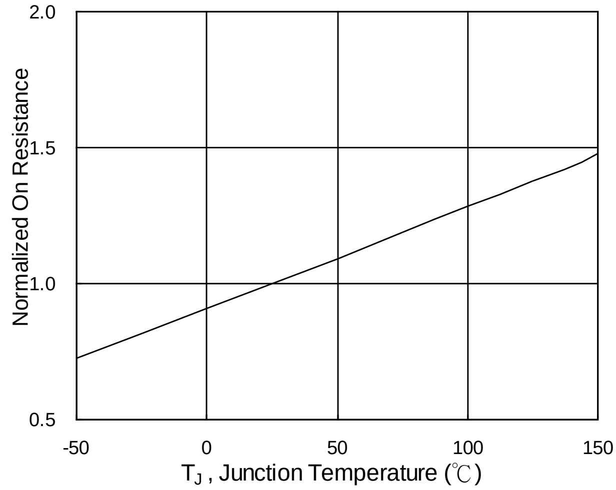


Fig.6 Normalized R_{DSON} vs. T_J

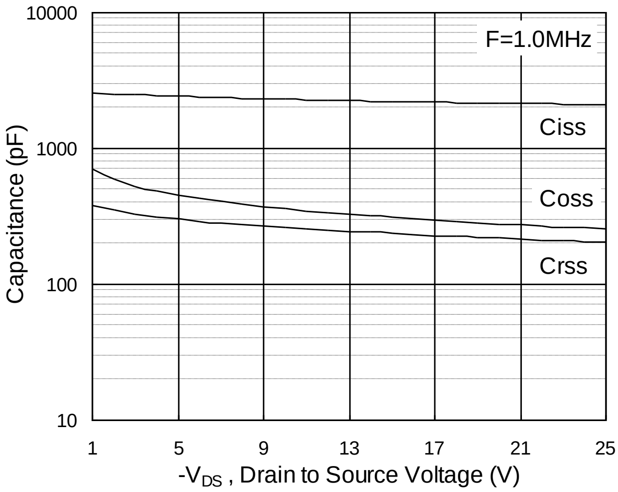


Fig.7 Capacitance

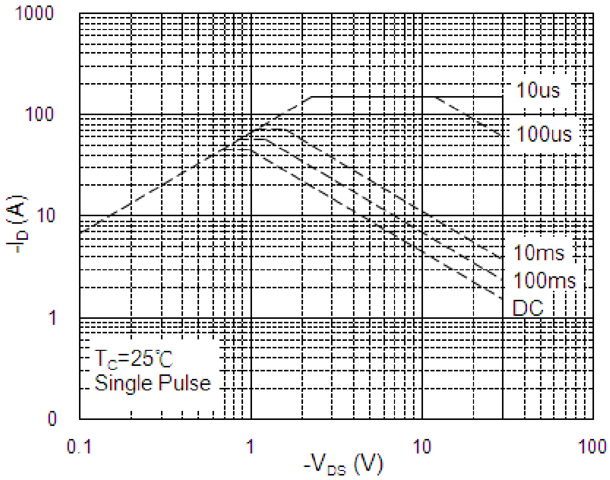


Fig.8 Safe Operating Area

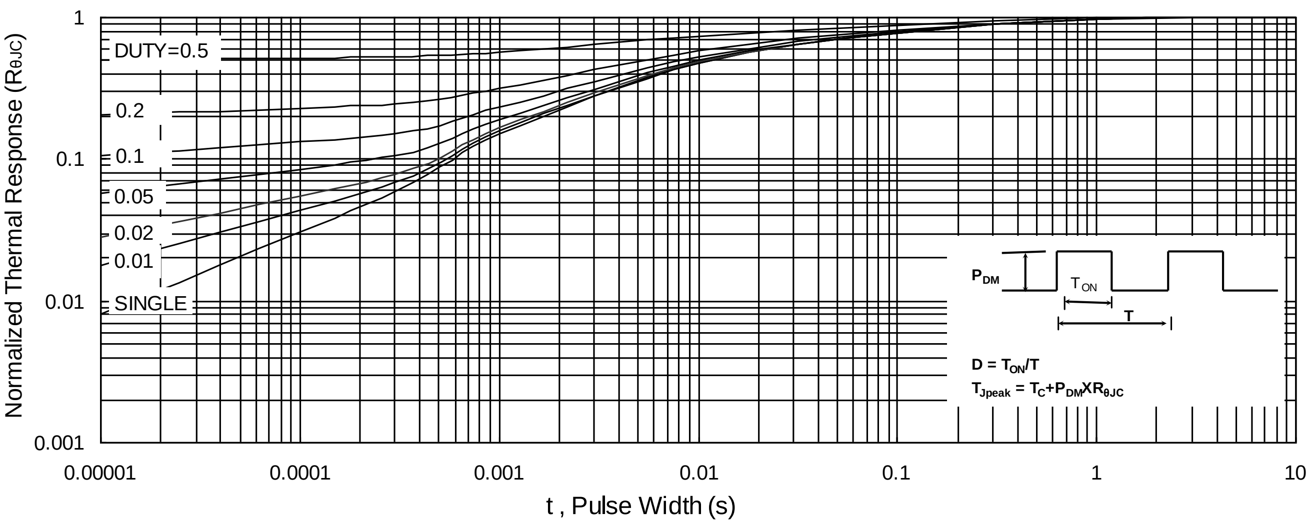


Fig.9 Normalized Maximum Transient Thermal Impedance

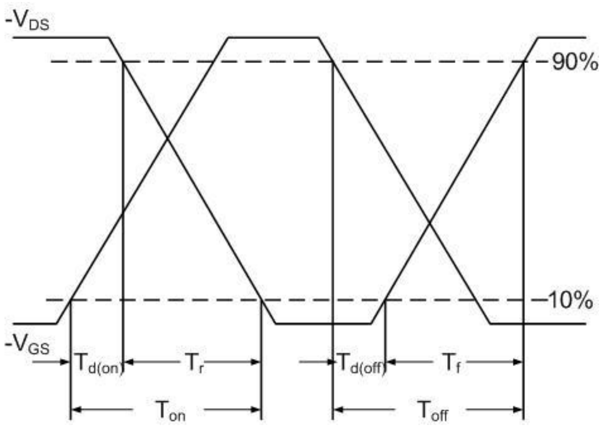


Fig.10 Switching Time Waveform

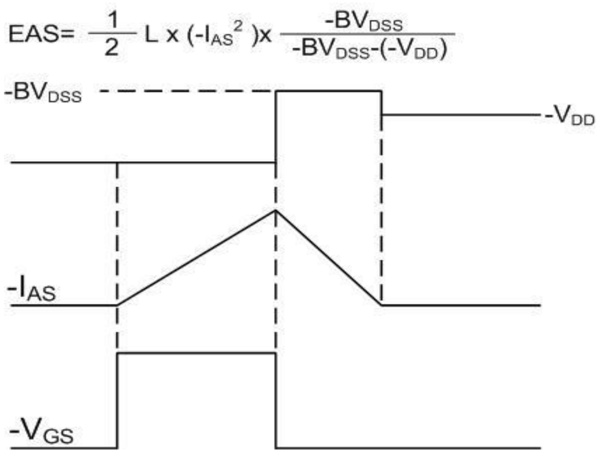
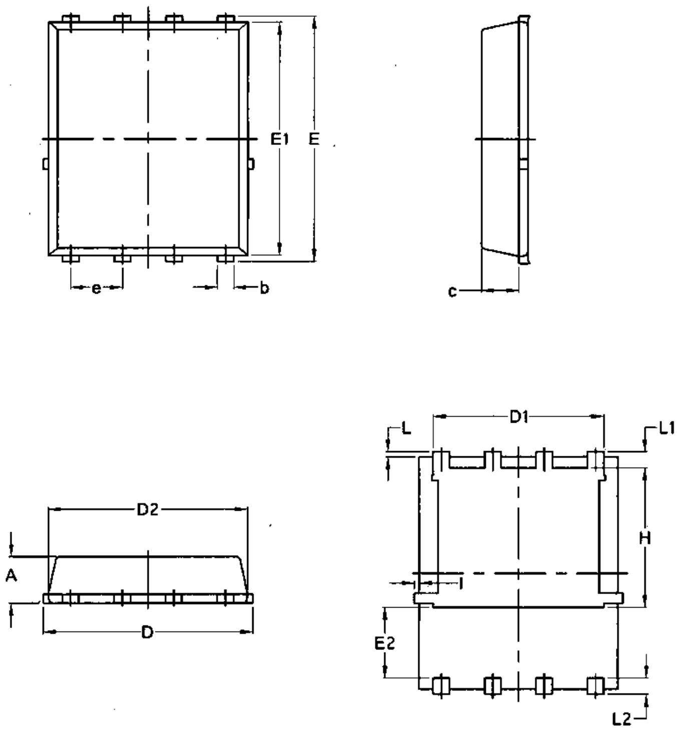


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-DFN5*6-8-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059