

**Description**

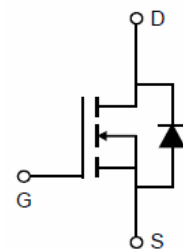
The LCE6005AR uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

**General Features**

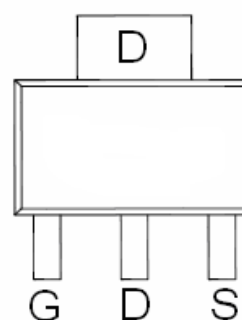
- $V_{DS}=60V, I_D=5A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS}=10V$  (Typ.26m $\Omega$ )  
 $R_{DS(ON)} < 45m\Omega @ V_{GS}=4.5V$  (Typ.32m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



SOT-223-3L view

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE6005AR	LCE6005AR	SOT-223-3L	Ø330mm	12mm	2500 units

**Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	5	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	3.5	A
Pulsed Drain Current	$I_{DM}$	24	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
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**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

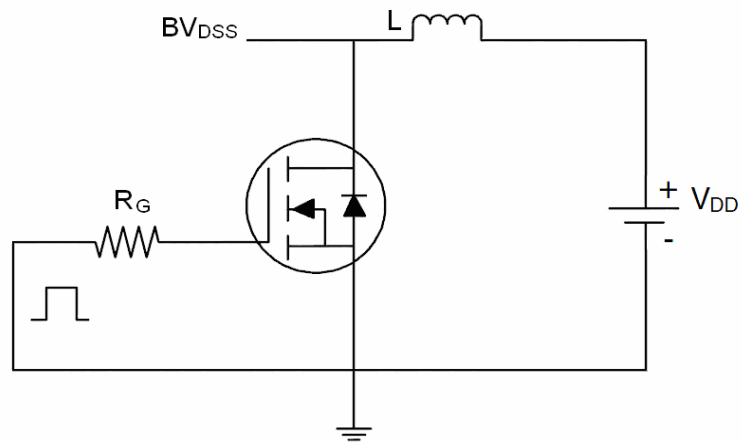
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-	26	35	mΩ
	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	32	45	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	11	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, F=1.0MHz	-	979	-	PF
Output Capacitance	C <sub>oss</sub>		-	120	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	100	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, R <sub>L</sub> =6.7Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	5.2	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	17	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	2.5	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	-	22		nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.3		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	5.2		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =5A	-		1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	5	A
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

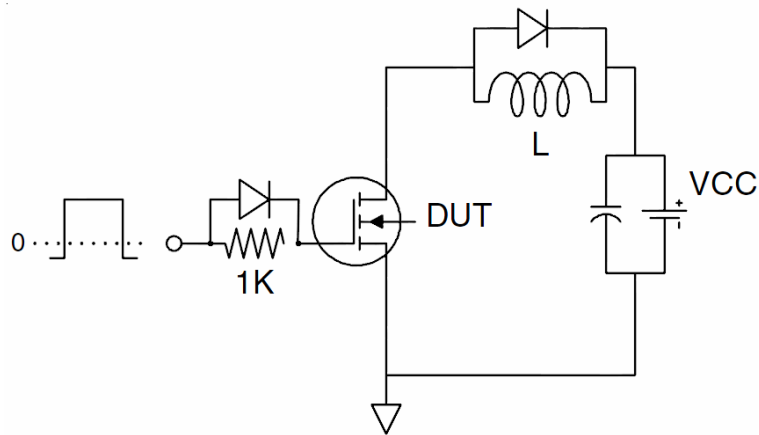
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω

### Test Circuit

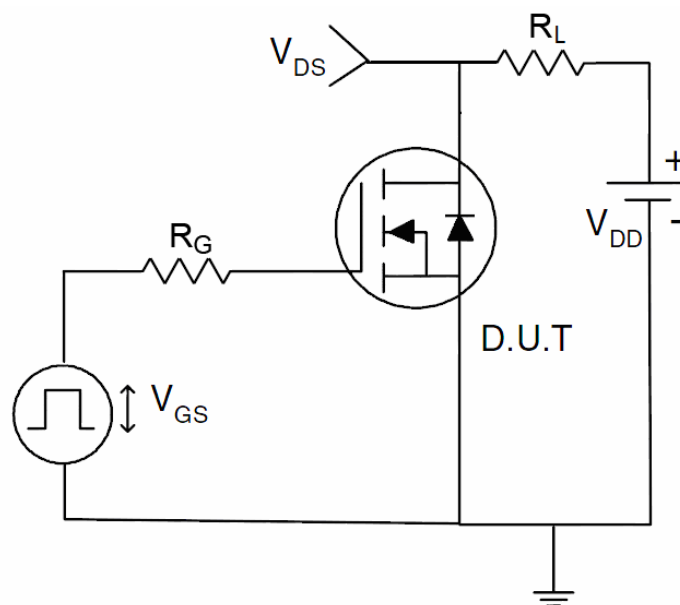
#### 1) E<sub>AS</sub> test Circuit



#### 2) Gate charge test Circuit



#### 3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

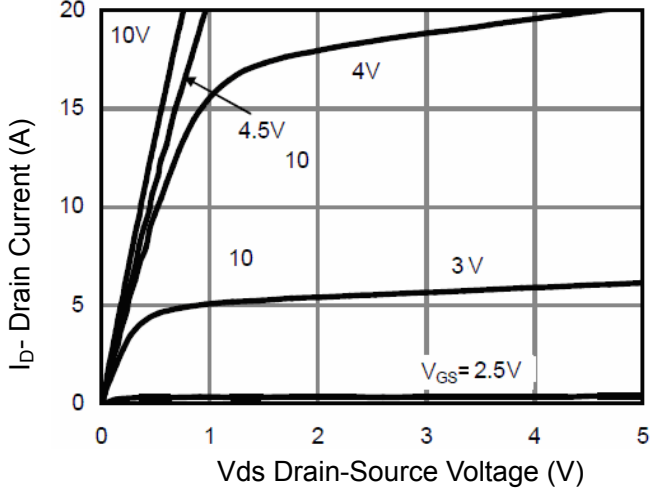


Figure 1 Output Characteristics

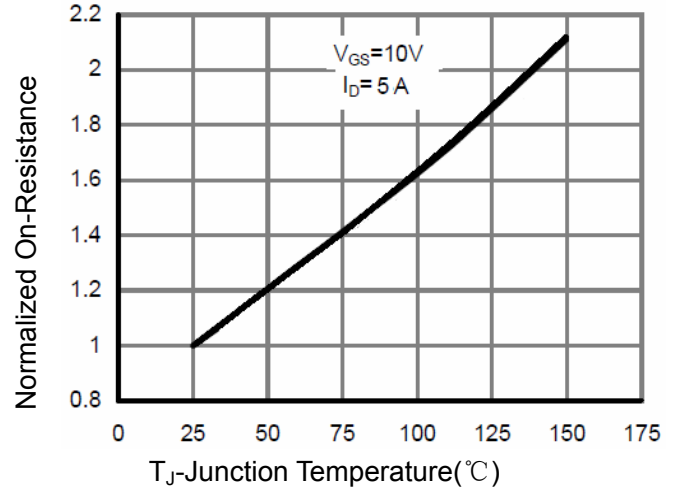


Figure 4 Rdson-Junction Temperature

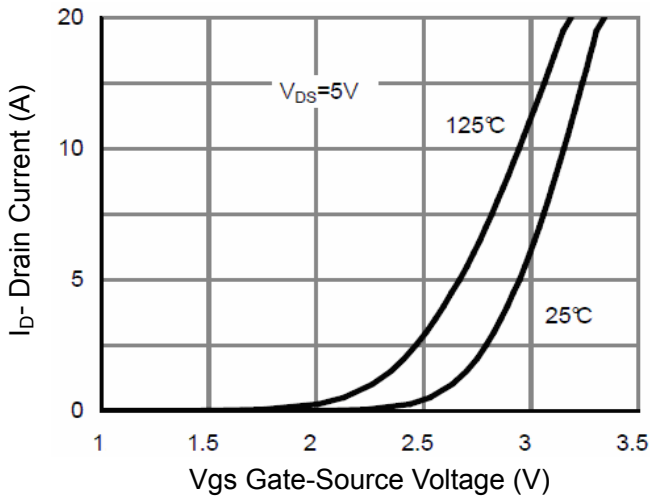


Figure 2 Transfer Characteristics

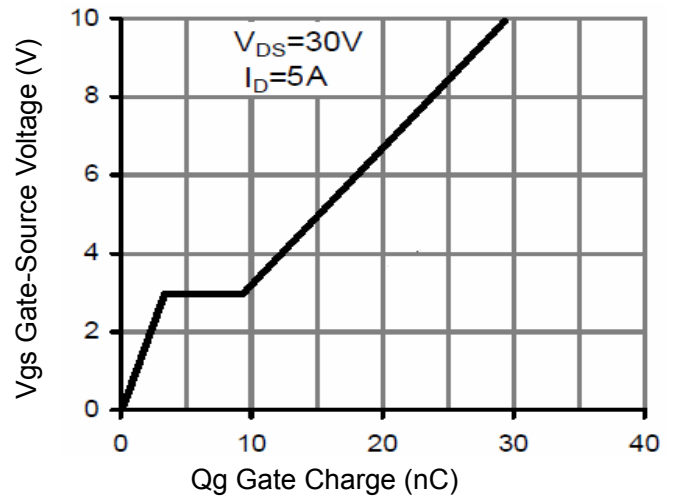


Figure 5 Gate Charge

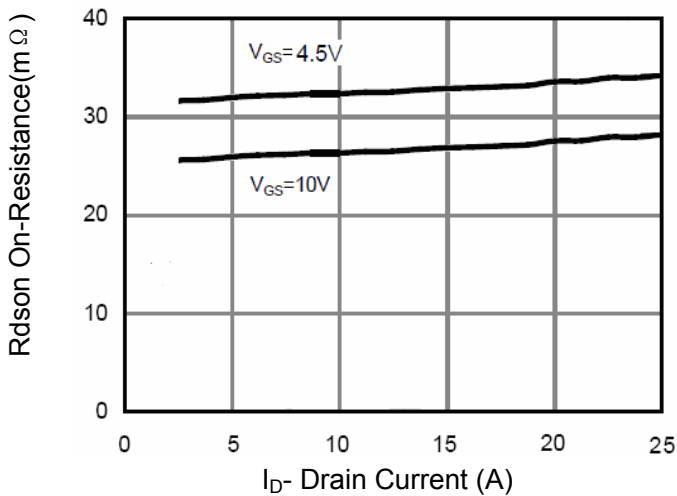


Figure 3 Rdson- Drain Current

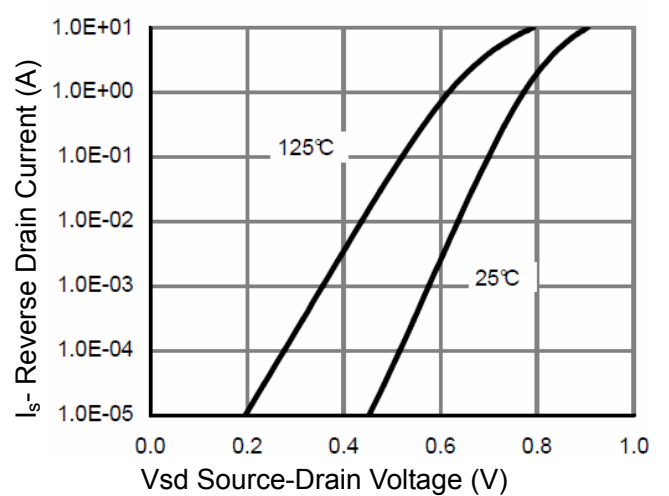


Figure 6 Source- Drain Diode Forward

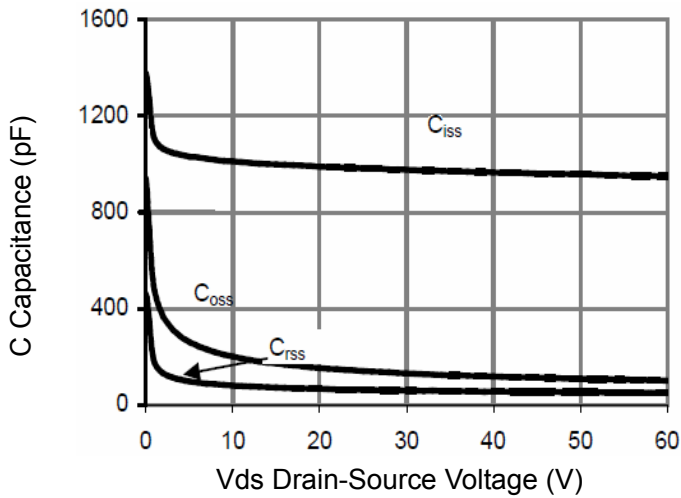


Figure 7 Capacitance vs Vds

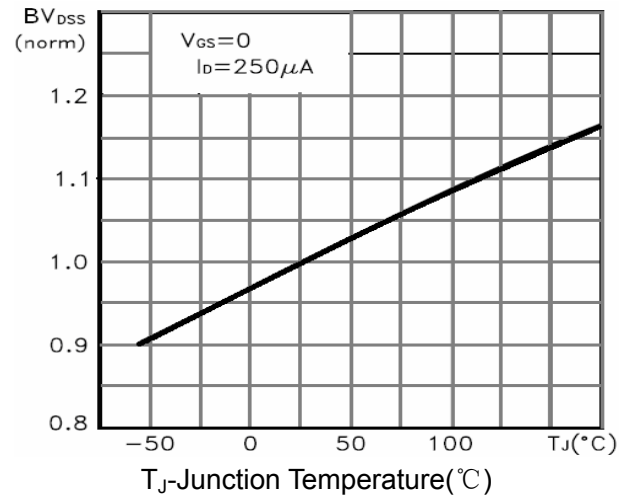


Figure 9  $BV_{DSS}$  vs Junction Temperature

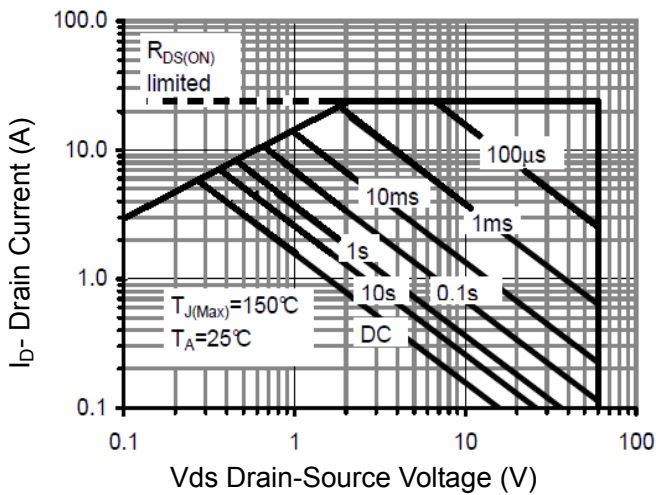


Figure 8 Safe Operation Area

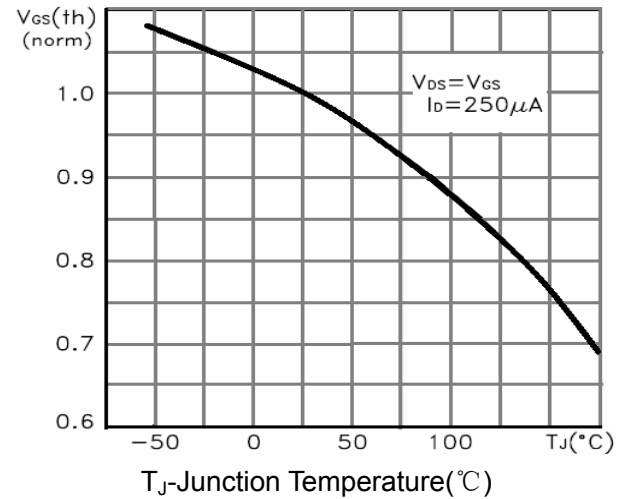


Figure 10  $V_{GS(th)}$  vs Junction Temperature

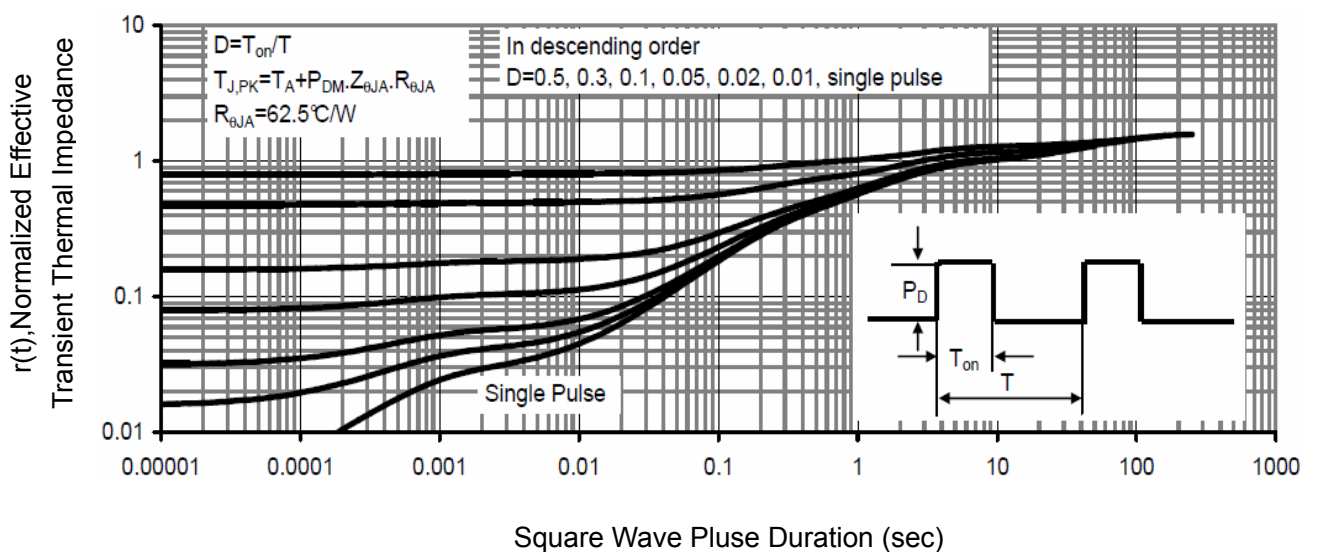
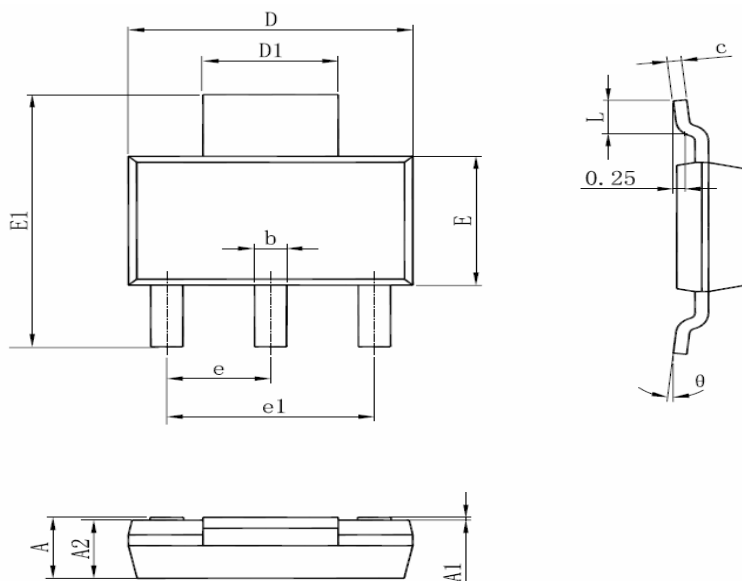


Figure 11 Normalized Maximum Transient Thermal Impedance



## SOT-223-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.520	1.800	0.060	0.071
A1	0.000	0.100	0.000	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.820	0.026	0.032
c	0.250	0.350	0.010	0.014
D	6.200	6.400	0.244	0.252
D1	2.900	3.100	0.114	0.122
E	3.300	3.700	0.130	0.146
E1	6.830	7.070	0.269	0.278
e	2.300(BSC)		0.091(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.150	0.035	0.045
$\theta$	0°	10°	0°	10°

## Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.